

FIG. 1a

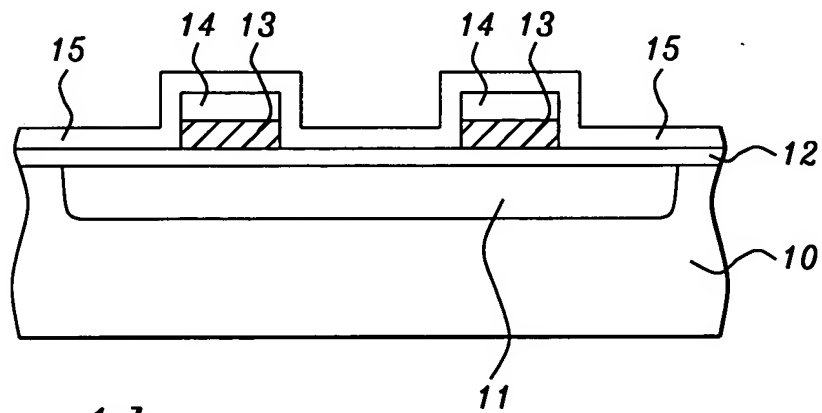


FIG. 1b

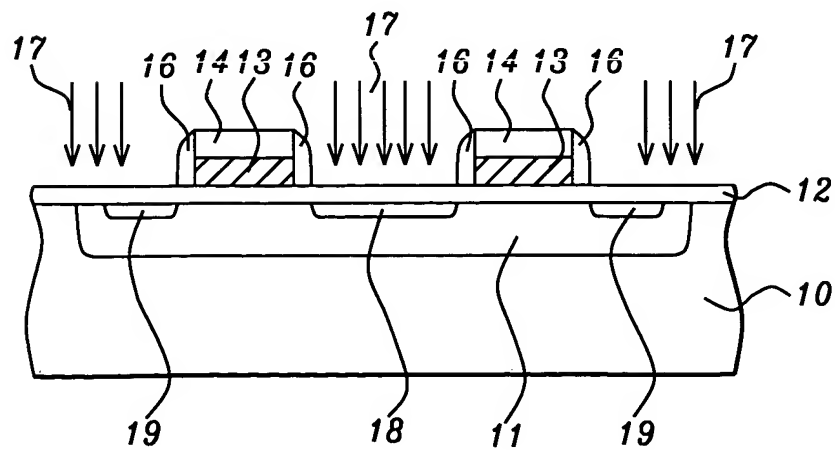


FIG. 1c

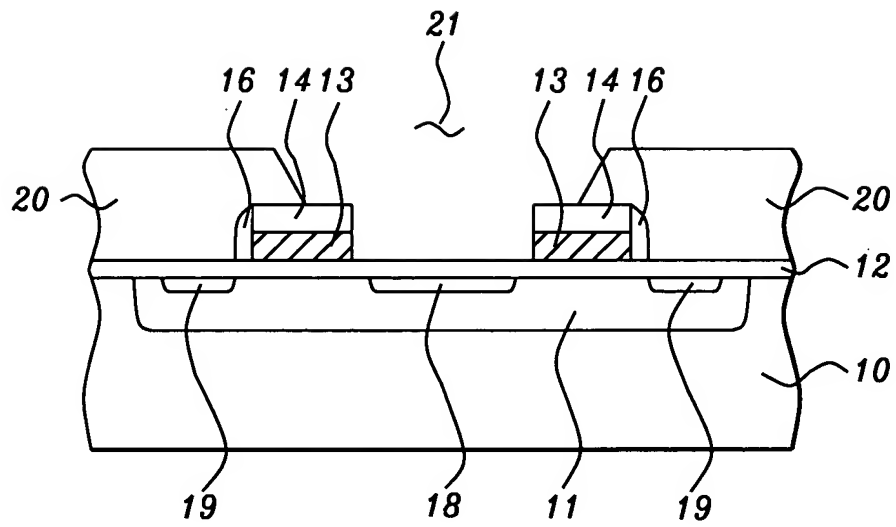


FIG. 1d

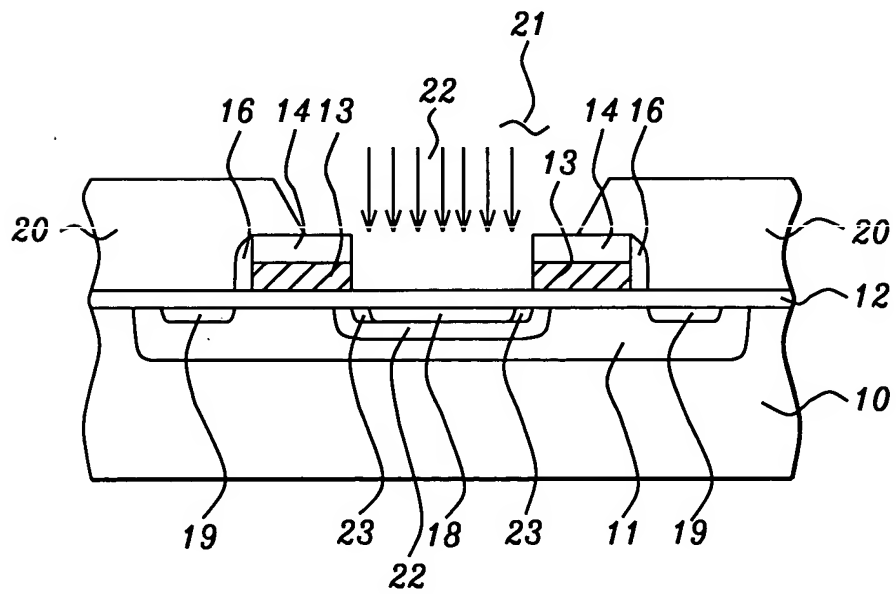


FIG. 1e

The diagram shows the timing for the PROGRAM operation. It features three word lines (WL) and five bit lines (BL). The word lines are labeled WL, WL, and WL from top to bottom. The bit lines are labeled BL, SL, BL, SL, and BL from left to right. The word lines are driven by a signal 41, which is a square wave with a high level at V_{dd} and a low level at 0V. The bit lines are driven by a signal 40, which is a square wave with a high level at V_{dd} and a low level at 0V. The word lines are also labeled with V_t and 0V. The bit lines are labeled with V_{dd} , 12V, 0V, 0V, and 0V. The diagram shows the timing of the word lines and bit lines during the PROGRAM operation.

FIG. 2a

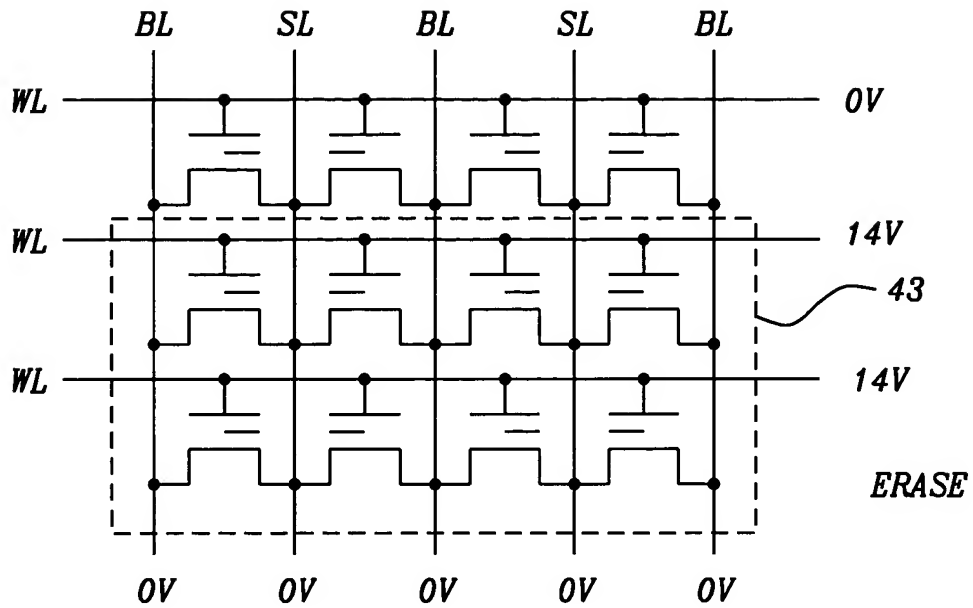


FIG. 2b

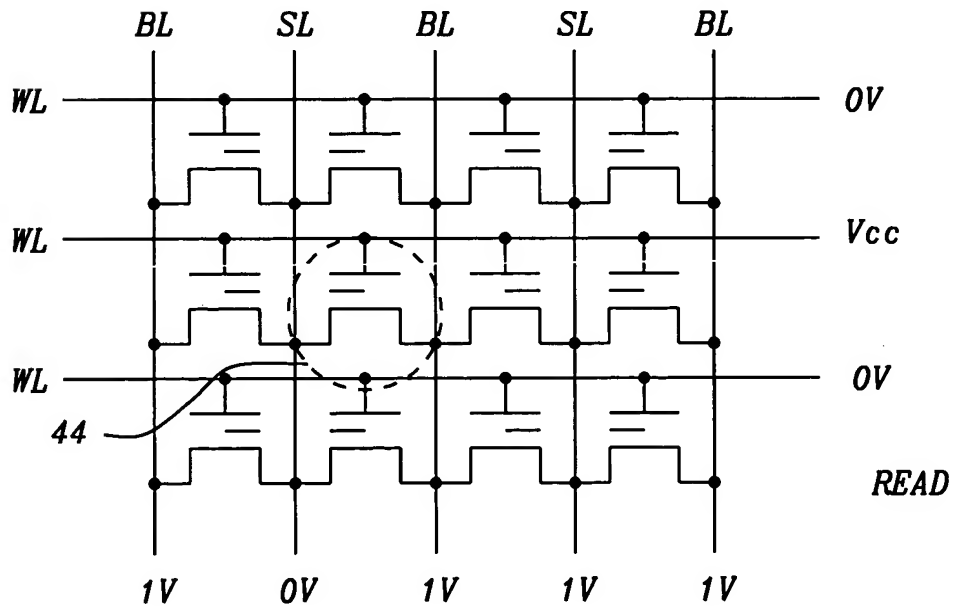


FIG. 2c

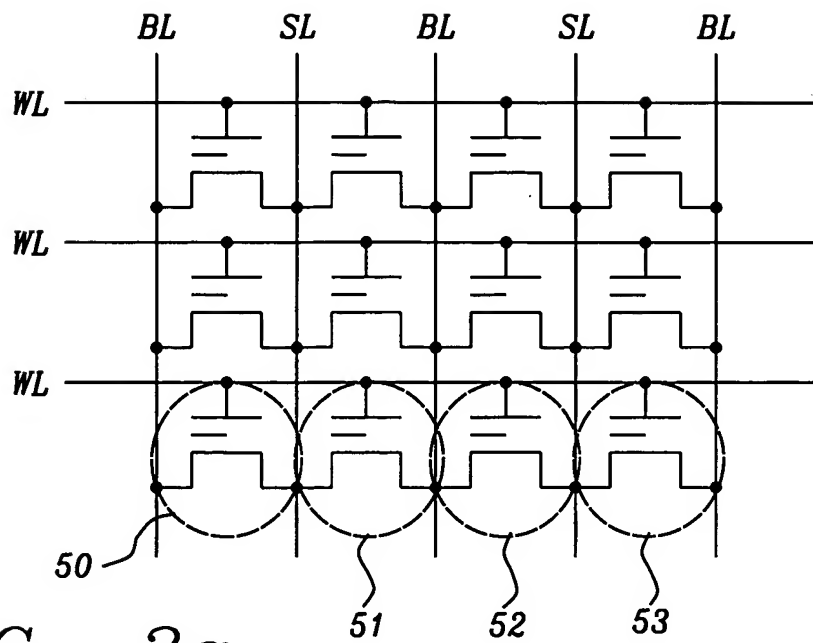


FIG. 3a

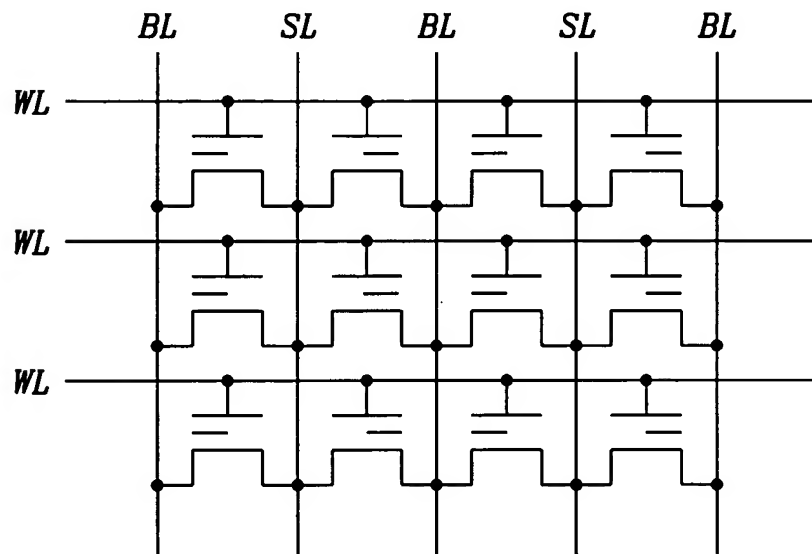


FIG. 3b

	WL	BL	SL
Program	V_t/Gnd	Gnd	12V
Erase	14V	Gnd	Gnd
Read	Vcc	1V	Gnd

FIG. 4